CBCS Scheme

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15NT54

Fifth Semester B.E. Degree Examination, Dec.2017/Jan.2018
Digital System Design

Time: 3 hrs. Max. Marks: 80

Note: ***Answer FIVE full questions, choosing one full question from each module.***

Module-1

1 a. Define combinational circuit. Design a full adder using truth table, kmap and draw the logic circuit for the full adder using XOR, AND, OR gates. **(10 Marks)**

b. Discuss the importance of HDL programming language and mention its advantages over C programming language. **(06 Marks)**

OR

2 a. Mention four types of descriptions in verilog HDL. Explain the behavioral and dataflow style with an example each. **(12 Marks)**

b. List the advantages of verilog HDL. **(04 Marks)**

Module-2

3 a. Realize a four bit Ripple Carry Adder using dataflow description in verilog with neat block diagram and output waveform. **(10 Marks)**

b. Derive Boolean equations for a two bit magnitude comparator. **(06 Marks)**

OR

4 a. Discuss in brief the importance of BCD to 7 segment display decoder. **(02 Marks)**

b. Implement a BCD to 7 segment driver (common cathode). **(14 Marks)**

Module-3

5 a. Design a 4-bit binary asynchronous ripple counter using T flip flop. Write the counting sequence and timing waveform. **(08 Marks)**

b. Define flip flop. Explain positive edge triggered JK flip flop using SR flip flop. **(08 Marks)**

OR

6 a. Explain the serial in-serial out (SISO) shift register. With a neat figure, also step by step with figure, show the transfer of 1011 till the last bit is output. **(08 Marks)**

b. Explain the 4 bit memory unit with address decoder. Also show the designed unit. **(08 Marks)**

Module-4

7 a. With a neat schematic, explain the CMOS inverter. **(07 Marks)**

b. Explain CMOS NAND gate with neat figure and truth table. **(09 Marks)**

OR

8 a. Explain 2 : 1 multiplexer using CMOS with relevant figures. **(08 Marks)**

b. Write a brief note on PMOS and NMOS transistors. **(08 Marks)**

Module-5

9 a. Write a verilog code for D-latch in dataflow description. Show the schematic and equation. **(10 Marks)**

b. Write a note on signal declaration and assignment statements in verilog. **(06 Marks)**

OR

10 a. Write a test bench / simulation module for a 4 bit ripple carry adder. **(08 Marks)**

b. Write a note on FPGA. **(08 Marks)**

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